

Description

Algo-Logic Systems' 40G TCP Endpoint implements a full TCP functionality in FPGA hardware that is capable of opening, maintaining, and closing TCP Connections. It has a receive-side ultra-low-latency of 96.0-nanoseconds.

Their network-tested TCP Endpoint delivers ultra-high performance and highest TCP bandwidth. It supports full duplex rates of 80 Gbps scalable to hundreds of Gigabits/second by using multiple ports within a single FPGA. Each port runs at the full 40G line rate.

The implementation runs on Altera Stratix V A-7 FPGA device and is compatible with all widely deployed FPGA platforms, including Solarflare AOE.

For datacenter acceleration, the 40G TCP Endpoint can be used for North-South data transfers inside racks from 40G/100G Top-of-Rack Switches. For datacenters configured with 40G East-West traffic pipes, the 40G TCP Endpoint will most efficiently transfer packets at full line-rate substantially increasing utilization while reducing Total Cost-of-Ownership (TCO).

Moreover, Algo-Logic's TCP Endpoint can be seamlessly integrated with OpenCL as well as Algo-Logic's other existing pre-built components in the low latency applications.

Algo-Logic provides engineering staff to ensure complete solution delivery with full support for end-system and application-level fastest time-to-market deployments.

Applications

- Streaming data analytics
- Datacenter acceleration
- Reliable messaging systems
- Network security appliances
- Storage appliances
- Backup appliances
- Bump-in-the-wire filtering systems
- Reliable, filtered feed redistribution
- Tick-to-Trade systems

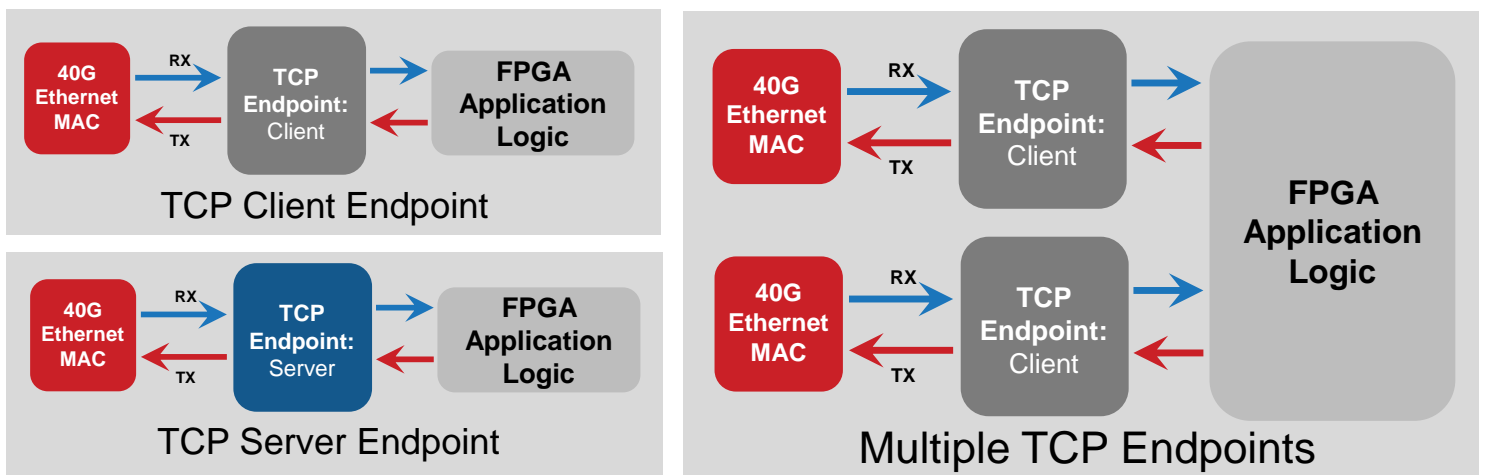
Key Features and Use-cases

- Ultra-low-latency purely RTL designed TCP/IP stack for layers 2, 3, and 4
 - Layer 1: IEEE802.3
 - Layer 2: IEEE802.3, ARP, VLAN
 - Layer 3: IPv4 and ICMP, IPv6 soon
 - Layer 4: TCP, UDP
- TCP retransmission buffer
 - Programmable buffer size, time out
 - Fast retransmit option
 - Programmable retransmission limit
- AXI-4 / Avalon streaming interface
- Cores running on Altera Stratix V A7 FPGA using multiple TCP Endpoints support hundreds of Gbps (duplex) of aggregated traffic
- OS independent, Web-based GUI or UDP network API for control and configuration
- High throughput option with large payloads up to 9,000 bytes (jumbo frames)
- TCP option support: MSS, window scaling, timestamps
- Robust flow control and error control
- Statistics for monitoring TCP sessions

40G TCP Endpoint Metrics

Ultra-low-latency	96.0 nanoseconds at 256 bits @ 156.25 MHz for 64 Byte packet
Default # Sessions Per Instance	32, 64, 128, 256, 512, 4K, and 16K
Processing Speed	40 Gbps line rate, scalable to 100 Gbps
Logic Footprint, Registers	4.4% ALMs in Stratix V A7, registers 1.4%
Memory Footprint (reconfigurable)	29% on-chip memory for 1024 KB buffer (reconfigurable)
FPGA Devices Supported	Stratix V A-7
Platforms Supported	Solarflare AOE

40G TCP Endpoint Configuration Options



Ordering Codes

AL-40G TCP – (Device) (Platform) (Ports) (Configuration) (Connection setup) (Retransmission buffer size)

Example:

- Device: Altera Stratix V A7
- Platforms: Solarflare AOE
- Ports: Number of 40GE Ports
- Configuration: Client Endpoint, Server Endpoint, Multiple Endpoints
- Connection setup: Automatic, pre-programmed
- Retransmission buffer size: e.g. 64KB