Ultra Low Latency 4th Generation 76-nanosecond TCP Endpoint

Description

The Algo-Logic Systems' U.S. exchange certified TCP Endpoint implements a full TCP functionality in FPGA hardware which is capable of opening, maintaining, and closing TCP Connections. It has an ultra low latency of 76-nanoseconds.

The mature, reliable, and network-tested Algo-Logic TCP Endpoint delivers ultra-high performance and highest TCP bandwidth. It supports full duplex rates of 20 Gbps scalable to 140 Gbps by using multiple ports within a single FPGA. It runs at the full Ethernet clock speed of 156.25 MHz enabling the core to run synchronously with the MAC and application specific processing logic.
The implementation is portable between Altera and Xilinx FPGA devices and compatible with all widely deployed FPGA platforms including Terasic DE5Net, Solarflare AOE, NetFPGA 10G, and other platforms.

Moreover, Algo-Logic's TCP Endpoint can be seamlessly integrated with all of Algo-Logic's existing pre-built components in the low latency application library (including pre-built protocol parsing libraries, market data filtering, and order processing). It can also be integrated with customer applications including pre-trade risk-checks, complete tick-to-trade applications, and algorithmic datacenter packet processing cores. Algo-Logic provides on-shore engineering staff to ensure complete solution delivery with full support for end-system and application-level fastest time-to-market deployments.

Applications

- High frequency trading
- Tick-to-Trade systems
- Pre-trade risk checks
- Reliable, filtered feed redistribution
- Trading/arbitrage opportunity discovery
- Proprietary/algorithmic trading strategies
- Financial surveillance systems

Key Features and Use-cases

- Ultra low latency purely RTL designed TCP/IP stack for layers 2, 3, and 4.
  - Layer 1: IEEE802.3
  - Layer 2: IEEE802.3, ARP, VLAN
  - Layer 3: IPv4 and ICMP
  - Layer 4: TCP, UDP
- TCP retransmission buffer
  - Programmable buffer size, time out
  - Fast retransmit option
  - Programmable retransmission limit
- AXI-4 / Avalon streaming interface.
- 76 ns ultra low latency proxy model enabling true parallel processing of client and server traffic.
- A single Altera Stratix V A7 FPGA using multiple TCP Endpoints supports 240 Gbps (duplex) of aggregated traffic to support 32-512, 4K, and 16K TCP sessions.
- OS independent, Web-based GUI or UDP network API for control and configuration.
- High throughput option with large payloads up to 9,000 bytes (jumbo frames).
- TCP option support: MSS, window scaling, timestamps.
- Robust flow control and error control.
- Statistics for monitoring TCP sessions.

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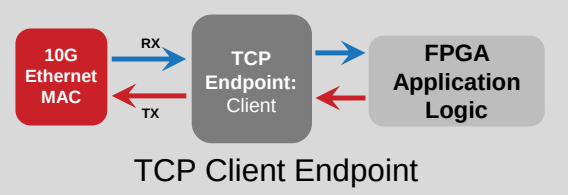
76-nanosecond TCP Endpoint

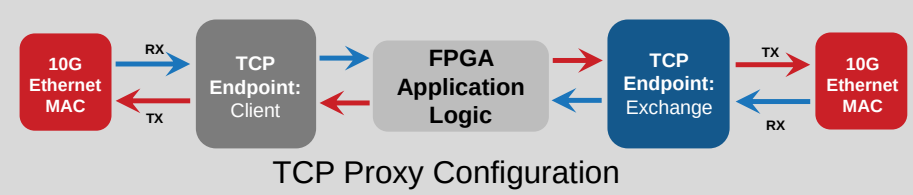
TCP Endpoint Metrics

Ultra Low Latency	76.8 nanoseconds at 156.25 MHz
Available # Sessions Per Instance	32, 64, 128, 256, 512, 4K, and 16K
Processing Speed	10 Gbps line rate, scalable to 40 to 100 Gbps
Logic Footprint	~3% ALMs in Stratix V A7
US-Exchange-Certified	Yes
FPGA Devices Supported	Stratix V, Virtex-7
Platforms Supported	Terasic DE5Net, NetFPGA10, Solarflare AOE, Nallatech P385, Bittware S5PH-Q

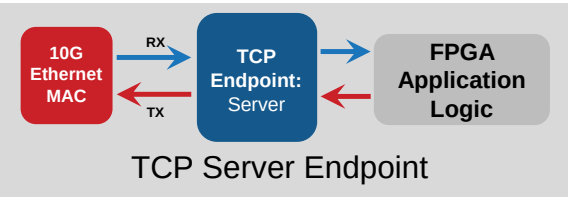
TCP Endpoint Configuration Options



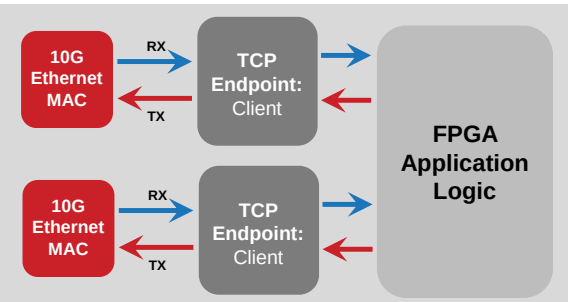
TCP Client Endpoint



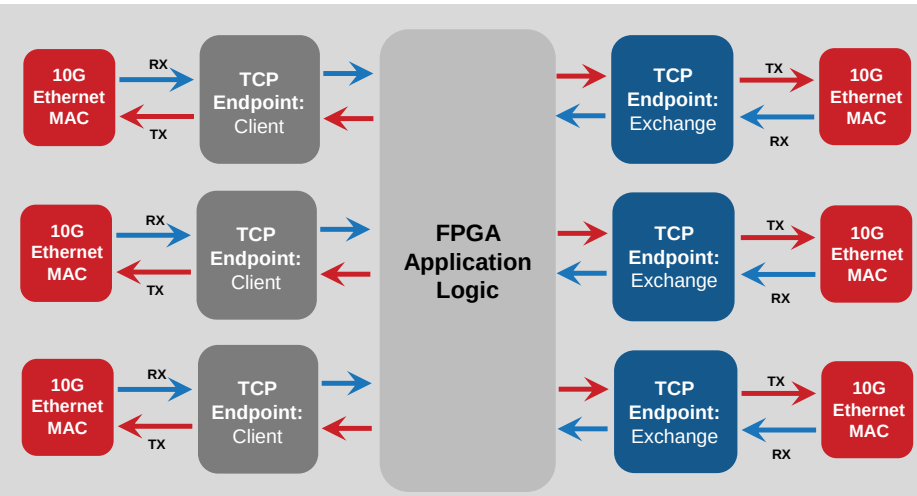
TCP Proxy Configuration



TCP Server Endpoint



Multiple TCP Endpoints



Multiple TCP Proxy Configurations

Ordering Codes

AL-TCP – (Device) (Platform) (Ports) (Configuration) (Connection setup) (Retransmission buffer size)

Example:

- Device: Altera Stratix V A7 / Xilinx Virtex 7
- Platforms: Terasic DE5Net, NetFPGA10, Solarflare AOE, Nallatech P385, Bittware S5PH-Q
- Ports: Number of 10GE Ports
- Configuration: Client Endpoint, Server Endpoint, Multiple Endpoints, Proxy Configuration, Multiple Proxy Configurations
- Connection setup: Automatic, pre-programmed
- Retransmission buffer size: e.g. 64KB

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