Ultra-Low-Latency 10GE PHY+MAC

Description

Having the lowest network latency is critical for Accelerated Finance. To achieve the lowest Ethernet latency, it is necessary to optimize the layer-1 PHY and the layer-2 MAC. Algo-Logic Systems' Ultra-Low-Latency (ULL) PHY+MAC minimizes roundtrip latency by several hundred nanoseconds as compared to vendor supplied IP cores. Algo-Logic Systems' ULL PHY+MAC design implements 10GBASE-R MAC and PCS (Physical Coding Sub-layer) functionality in an FPGA by using logic optimized for latency.

The ULL PHY+MAC is compatible with multiple FPGA platforms that support SERDES rates of 10.3125 Gbps while bypassing all PCS and excessive buffering features. The MAC interfaces to user logic via the 64-bit Avalon-ST bus or AXI4-Stream standards.

The Ethernet Frame Check Sequence (FCS) within the transfer is automatically added in the transmit direction; the FCS is checked, indicated, and removed in the receive direction. The only padding done is on the transmit side (Tx) if the transmitter MAC sees fewer than 60 bytes. On the receive side (Rx), the MAC passes the packet that it receives without change.

In this fashion Algo-Logic Systems' ULL PHY+MAC is designed to seamlessly replace much slower default PHY+MAC implementations that come with standard FPGA platforms.

Applications

- High Frequency Trading (HFT)
  - Market makers, trading firms, stock exchanges
- High-performance datacenter networks
  - Enables world's fastest key/value search over Ethernet
- Real-time Internet data collection

Key Features

- 89ns round-trip (fiber-to-fiber or gate-to-gate) for 10 Gigabit Ethernet, first-bit to first-bit
- Reconciliation sub-layer implementation compliant with IEEE802.3
- Local fault and remote fault detection and handling
- Frame Check Sequence (FCS) insertion and verification at line rate
- Automatic transmit padding, jumbo frame support, transmit and receive statistics counters
- Compatible with multiple FPGA platforms as soft-logic around SERDES
  - Supports both standard Avalon-ST / AXI4-Stream bus interfaces
  - Direct replacement for high-latency default vendor cores
- High level architecture Ethernet MAC design is flexible in its use of system clock (on the Avalon ST side)
- Low gate count (1,271 ALMs on Stratix V)
- Includes support for 1Gbps Ethernet

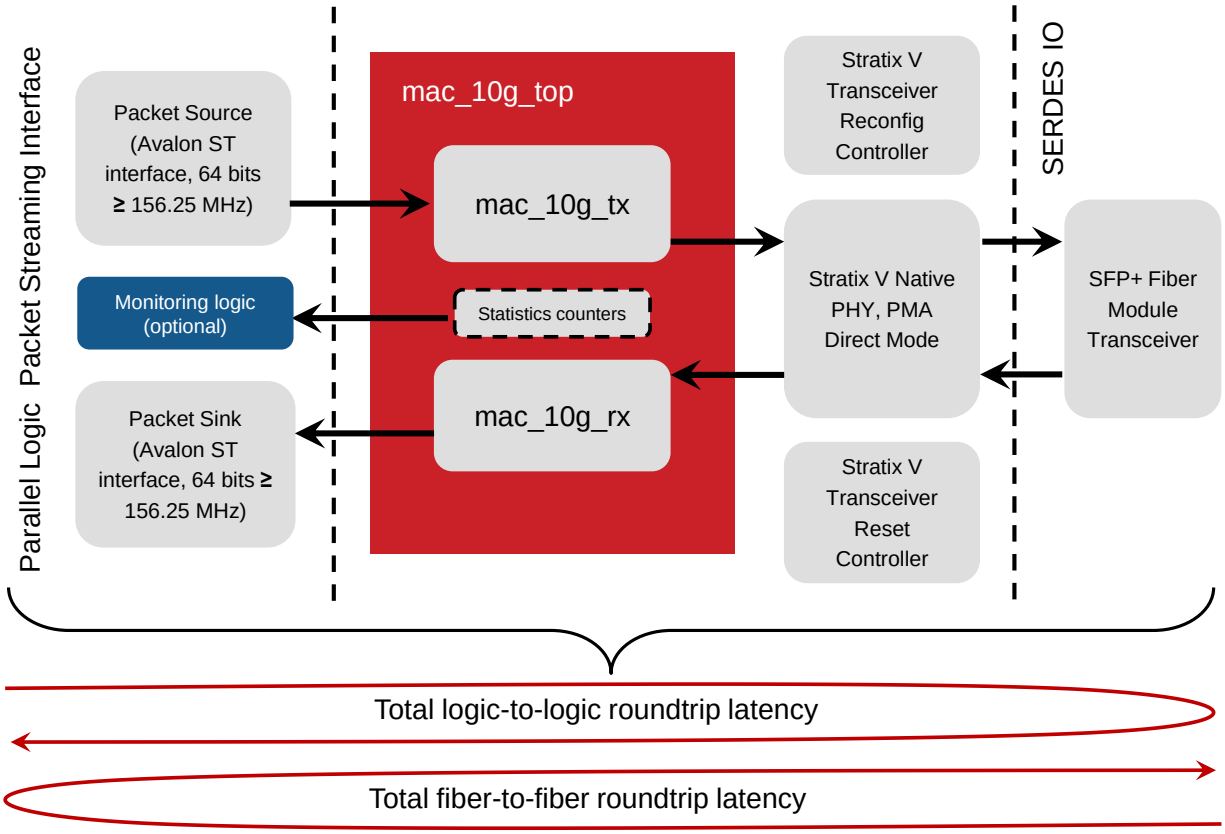
www.algo-logic.com
Solutions@Algo-Logic.com
+1 (408) 707-3740

Ultra-Low-Latency 10GE PHY+MAC

Ultra-Low-Latency PHY+MAC Metrics

Total 10GE PHY+MAC Rx + Tx Roundtrip Latency *(including clock-crossings with logic at 161MHz and faster)*	74.5 nanoseconds roundtrip fiber-to-fiber, Tx = 0, Rx = 0
Total 10GE PHY+MAC Rx + Tx Roundtrip Latency *(including clock-crossings and playout buffer to logic at 156.25MHz)*	89.6 nanoseconds roundtrip fiber-to-fiber
Processing Speed Models	10 Gbps line rates
Jumbo Frame Support	Up to 16,000 Bytes
FPGA Devices Supported	Altera Stratix® V and Xilinx UltraScale®
FPGA Platforms Supported	Terasic DE5Net, SolarFlare AOE, Nallatech P385, Bittware S5PH-Q, PLDA

Ultra-Low-Latency PHY+MAC Diagram



Ordering Codes

ULL-PHY+MAC: (Device) (Line rate) (Platform) → Example:

- Device: Altera, Xilinx
- Line rate: 10Gbps
- Platform: Terasic DE5Net, SolarFlare AOE, Nallatech P385, Bittware S5PH-Q, PLDA Xpress GXSLP

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