Ultra Low Latency 10GE PHY+MAC

AOE FDK Platform

Description

Achieving the lowest network latency is critical for Accelerated Finance. To obtain the lowest Ethernet latency, it is necessary to optimize the layer-1 PHY and the layer-2 MAC. Algo-Logic Systems' Ultra Low Latency (ULL) PHY+MAC reduces roundtrip latency by several hundred nanoseconds as compared to vendor-supplied IP cores.

The ULL PHY+MAC design implements 10GBASE-R MAC and Physical Coding Sub-layer (PCS) functionality in an FPGA by using logic optimized for latency.

The combined solution of Algo-Logic's ULL PHY+MAC and Solarflare AOE2 Firmware Development Kit (FDK) card allows the client to easily program logic into the FPGA User RTL block with ultra low latency networking.

The integrated platform supports:

- 2 Configurable ULL PHY+MAC bundles on the line side (up to 8 x 10GE via 2 QSFP+ ports)
  - Each bundle allows up to 4 ULL PHYs + MACs
- 2 x 10GBASE-R on the Solarflare ASIC NIC interface
- SERDES rates of 10.3125 Gbps
- MAC interface to user logic via the 64-bit Avalon-ST bus standard (supports clock crossing)

The Ethernet Frame Check Sequence (FCS) is added in the transmit direction, and then checked and removed in the receive direction. Padding is optionally done on the transmit side (Tx) if the MAC sees fewer than 60 bytes. On the receive side (Rx), the MAC passes the received packet without change.

Applications

- High Frequency Trading (HFT)
  - Market making, trading, exchanges, A/B arbitration
- High-performance datacenter networks
  - Port fanout, relay, packet processing

Key Features

- 89ns round-trip delay through the 10GE PHY+MAC + (Tx + Rx) SERDES (fiber-to-fiber or gate-to-gate) first-bit to first-bit
- Small footprint with low gate count of 1,331 ALMs on Stratix V per 10GE MAC
- Frame Check Sequence (FCS) insertion and verification at line rate
- Automatic transmit padding
- Jumbo frame support
- Transmit and receive statistics counters
- Ethernet MAC provides flexibility to use of system clock on Avalon ST side at 156.25MHz - 200MHz
- Reconciliation sub-layer implementation compliant with IEEE 802.3

Solarflare AOE2 card

www.algo-logic.com
Solutions@Algo-Logic.com
+1 (408) 707-3740

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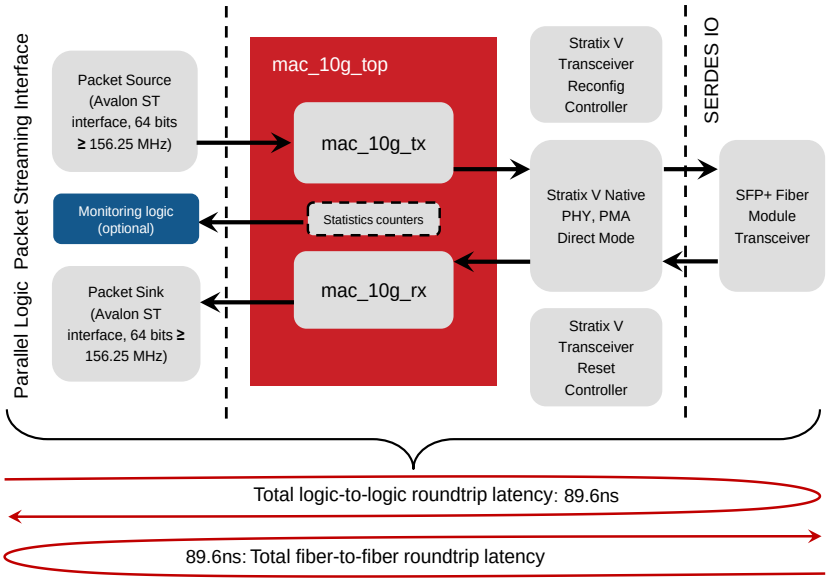
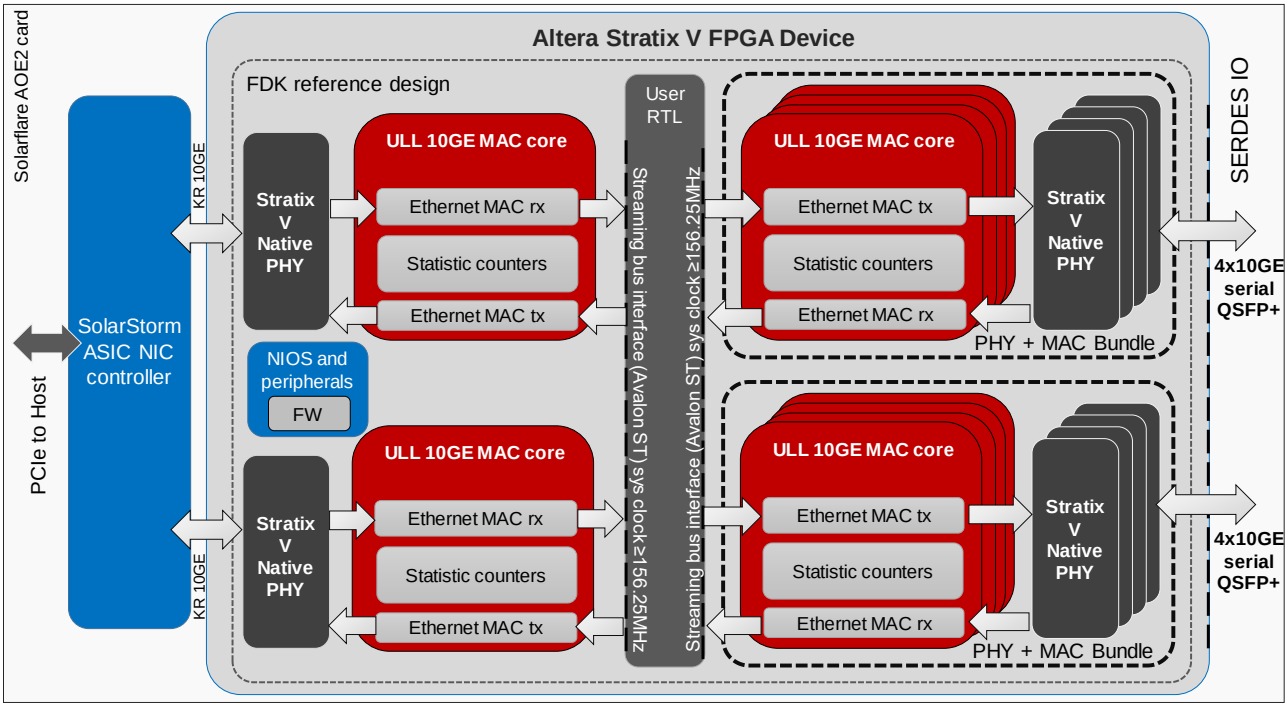
Ultra Low Latency PHY+MAC Metrics and Measurement Diagram

Total 10GE PHY+MAC Rx + Tx Roundtrip Latency *(including clock-crossings and playout buffer to logic at 156.25MHz)*	89.6 nanoseconds roundtrip (fiber-to-fiber)
Throughput	Continuous 10 Gbps line rate
Jumbo Frame Support	Up to 9,000 Bytes
FPGA Platform and Device	Solarflare AOE2, Altera Stratix® V 5SGXMA7K2F40C2N (A7C2)
Single MAC Logic Utilization (in ALMs)	1,331/234,720 (<0.57%)



Ultra Low Latency PHY+MAC on Solarflare AOE2 Card Diagram



Ordering Codes

ULL-PHY+MAC: (Device) (Line rate) (Platform)

Algorithms in Logic

www.algo-logic.com
Solutions@Algo-Logic.com
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