# Network Processing in Reconfigurable Hardware

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## Technology Options for Network Processing

<table>
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<tr>
<th>Technology</th>
<th>Features</th>
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| **Microprocessors**         |  ✓ Fully Reprogrammable  
                            |   o Optimized for general purpose computing  
                            |   o Sequential Processing  |
| **Custom Packet Processing Hardware** |  ✓ Highly concurrent processing  
                            |   ✓ Optimized for specific networking application  
                            |   o Static Functionality  |
| **Network Processors**      |  ✓ Fully Reprogrammable  
                            |   ✓ Some concurrent processing (8-32 cores)  
                            |   ✓ Some hardware optimized for applications  |
| **Reconfigurable Hardware** |  ✓ Fully Programmable  
                            |   ✓ Highly concurrent processing  
                            |   ✓ Hardware optimized for specific application  |
Properties of Ideal Network Processor

- **High Performance**
  - Fast Network Interfaces
    - OC48 (2.4 Gbps) and better
  - Hardware Accelerated
    - 10 Million packets/second +

- **Fully Extensible**
  - Fully Programmable
  - Modular Plugins

- **Open Interfaces**
  - Open switch interface
    - Device fits into existing switch and firewall
  - Open hardware interface
    - FPGA modules can be added and combined
  - Open software and signaling interfaces

Field Programmable Port Extender (FPX)
FPX in Washington University Gigabit Switch

Using FPX & WUGS Process and Route Packets

Fast Ethernet Switch w/Fiber uplink

PC

Internet

PC

PC

PC

PC
FPX “in a box” Firewall Configuration

Fast Ethernet Switch w/Fiber uplink

Fiber uplink To backbone switch (Fore PH 8000)

Internet

FPX Platform platform developed

FPX combined with WUGS to route and process Internet packets
Properties of a Module

Payload Processing Environment

- Network applications benefit from higher-level data abstractions
- Protocol Wrapper Framework provides a simple interface to multiple layers of a Network
Layout of typical FPX Hardware Module

Packet Processing Hardware

- UDP/TCP Processor
- IP Processor
- Frame Processor
- Cell Processor

Content-Aware Firewall on a Chip

Layered Protocol Wrappers

(Implemented on the RAD on the FPX, using a VirtexE 2000 FPGA)
**DHP Implementation on the FPX**

- **Reprogrammable Application Device (RAD)**
  - Circuit on XCV2000E
  - SRAM and SDRAM Interfaces
  - Control Cell Processor
  - Holds 2+ DHP Modules
  - Reprogrammable over network

- **Network Interface Device (NID)**
  - XCV600E FPGA
  - Controls FPX
  - Full packet switch with per-flow routing
  - Controls bitstream cache
  - Programs RAD over net

**Floorplanning - Sample Infrastructure**

- **DHP RESERVED AREAS**
### Other Modules Implemented

- **IPv6 Tunneling Module**
  - Tunnels IPv6 over IPv4

- **Statistics Module**
  - Event counter

- **Traffic Generator**
  - Per-flow mixing

- **Video Recoder**
  - Motion JPEG

- **Embedded Processor**
  - KCPSM

- **IPv4 CAM Filter**
  - 104 Bit header matching

- **Fast IP Lookup (FIPL)**
  - Longest Prefix Match
  - MAE-West at 10M pkts/second

- **Packet Content Scanner**
  - Reg. Expression Search

- **Data Queueing**
  - Per-flow queue in SDRAM

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### Control and Reconfiguration
Reprogramming the FPX

(1) New Module is created

2) The full or partial bitstream is sent over network to the NID on the FPX and stored in the configuration cache

(3) A Command Issued to reconfigure hardware

(4) NID Reads Memory and reprograms RAD via SelectMAP

Reconfiguration Times

- **Million-Gate Reconfiguration (XCV2000E)**
  - Configuration Size: 1.25 Mbytes = 10 Mbits
  - Network Transfer: 10 Mbit / 1 Gbps = 10ms
  - Configuration Time: 1.25 Mbyte / 50 MHz = 25ms

- **Hardware Plug-in Module Reconfiguration**
  - Configuration Size: 200 Kbytes = 1.6 Mbits
  - Network Transfer: 1.6 Mbit / 1 Gbps = 1.6 ms
  - Configuration Time: 200 Kbytes / 50 MHz = 4ms
Control and Configuration Services

- Allows communication to FPX hardware over the Internet using the Web, TCP/IP Sockets, or other signalling packages.

- Provides API to controls and configures the FPX

- Provides reliable transport mechanism with retransmission to communicate with hardware

- Allows multiple control devices to remotely connect and control common FPX resources

Control and Configuration GUI

- Web interface to communicate with the FPX

- Menu Functions
  - Route traffic flows
  - Reprogram hardware
  - Upload bitfiles
  - Read & write on-chip Memory
  - Create test cells
Installation of New Hardware Module

- Allows uploading and downloading of full or partial bitfiles
- Allows user to select a bitfile for programming
- FPGA reconfigures when user presses ‘Execute Command’

Summary

- Reconfigurable Hardware performs Network Processing
  - Provides high degree of configurability
    - Literally, every gate of a module can be reprogrammed
  - Provides high performance
    - OC48 (2.4 Gbps) performance achieved using Xilinx XCV2000E-6
- Field Programmable Port Extender (FPX) Platform Developed
  - 85 FPX devices built
  - Over 20 Hardware modules have been developed
- Layered Internet Protocol wrappers
  - Enable processing Internet packets at Gigabit rates
- Control and Reconfiguration Mechanisms
  - Hardware Modules dynamically reconfigure over the network
  - Control software provides extendable socket interfaces
  - Web interface simplifies FPX control and configuration
  - Chained TCP/IP channel simultaneously programs multiple FPX devices