

Description:

Algo-Logic's low latency PCI express (PCIe) solutions rapidly transfer data between Field Programmable Gate Array (FPGA) logic, processors, and memory. For example, in many High Frequency Trading (HFT) systems, rapid data transfers are needed between FPGA logic and the Order Management System (OMS) software. For these frequent and short transactions, Algo-Logic's PCIe solutions are optimal for minimizing latency.

Similarly, in datacenter applications, PCIe solutions typically interface processors with network and storage devices. Algo-Logic's PCIe solutions and Ethernet IP cores are used in high performance Network Attached Storage (NAS), Storage Area Networks (SAN), and Key-Value Store (KVS).

Algo-Logic's PCIe solutions are plug-and-play; the hardware interfaces and software APIs are easy to use for software developers building low latency network streaming applications.

The Register Interface supports a low latency host to FPGA communication through memory-mapped I/O (MMIO) with write combining. The Direct Memory Access (DMA) Engine is specifically designed for kernel-bypass Linux applications that require high throughput and low latency. The DMA Engine functions include:

- I. Data transfer to implement zero-copy ring buffers memory mapped to userspace
- II. FPGA that advertises data arrival to the descriptor ring buffer
- III. Software API that polls from the descriptor ring buffer to detect data arrival, size, and location in the ring buffer

Applications and Use-cases:

- Low latency applications
- High Frequency Trading (HFT)
- High Performance Computing (HPC)
- Heterogeneous computing with FPGA logic and host software
- Compute and storage applications
- Low latency kernel bypass network interface
- FPGA Endpoint

Key Features:

- Easy to use C/C++ API
- Parallel tasking support for multiple threads
- Four independent Tx/Rx interfaces
- Standard Avalon streaming interface for seamless integration with network logic
- DMA Engine provides fastest transfer of data from FPGA logic to software
- Polling and Ring Buffer DMA architecture
- Gen 3 with backward compatibility to Gen 2

Compatible Hardware Platforms

- Tested with multiple hardware platforms, including the Intel i7 and Xeon processors
- Pre-programmed gateway application on a half-height or full-height expansion card that fits into any standard x86 Linux server
- Commercially available Altera FPGA platforms including Stratix V and Arria-10 devices

Software APIs

- Client software compatible with Red Hat and CentOS with C/C++ APIs
- Free, open source Apache 2 software license

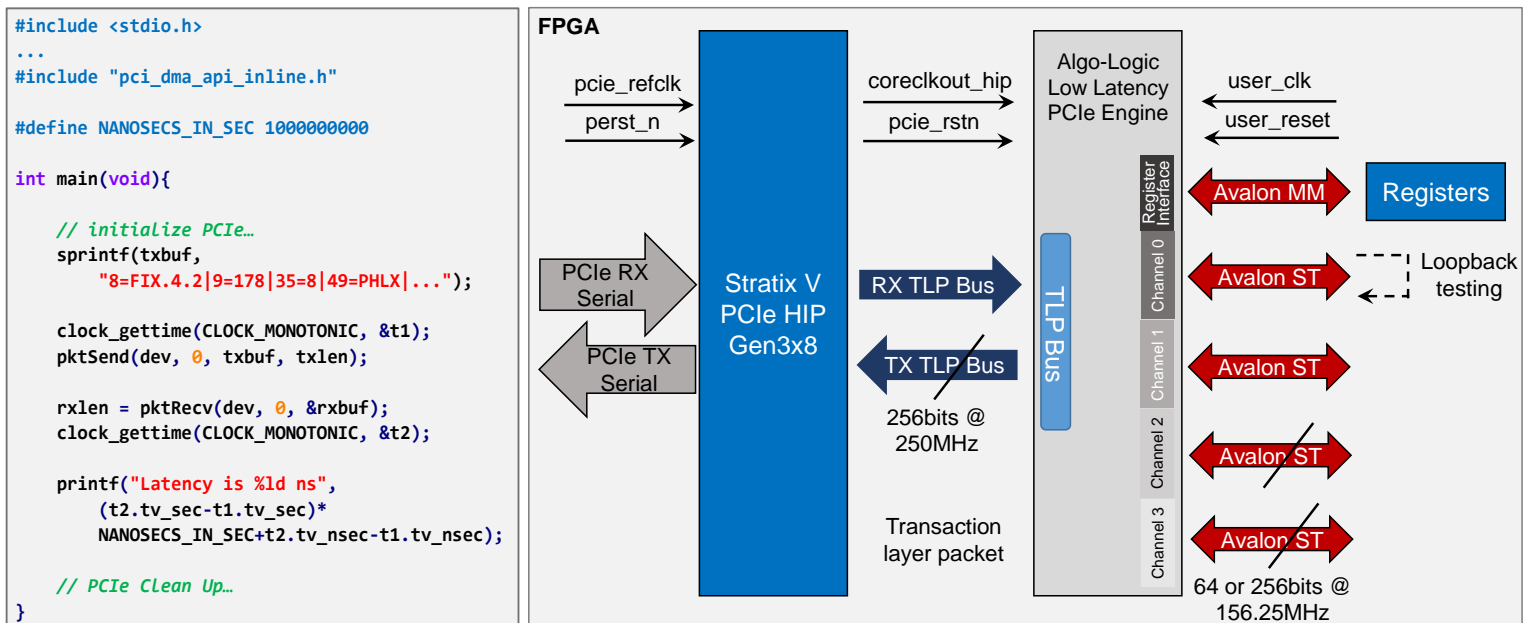
GDN-PCIe Solutions Metrics:

PCIe Support Types	Generation 3 x8
Number of DMA Channels	4
Median Latency Host to FPGA RT	1 microseconds for 300 Byte datagram*
P99 Latency Host to FPGA RT	1.26 microsecond for 300 Byte datagram*
Throughput – Host to FPGA	Up to 27 Gbps*
Throughput – FPGA to Host	> 40 Gbps*
FPGA Devices Supported	Altera Stratix V, Arria-10

* Test configuration: 256 bit wide bus at 156.25Mhz clock domain on Intel i7 at 3.5Ghz

GDN-PCIe Round Trip Latency Diagram:

Software developers can easily communicate with FPGA hardware using the short code below.



Ordering Codes

AL-PCIe Gen 3x8 – (Device) (Ports) (Connection Setup) (Reference Platform)

Example:

- Device: Altera
- Ports: Number of Avalon streaming ports
- Connection Setup: Automatic, pre-programmed
- Reference Platforms: Terasic DE5-Net, Nallatech P385